REMARKS

Claims 3 and 6 are amended. Claims 1-14 remain in the Application. Reconsideration of the pending claims is respectfully requested in view of the above amendment and the following remarks.

I. Claims Objections

Claims 3 and 6 are objected to because of informalities. As requested by the Examiner, Applicants amend Claim 3 to replace "a second three-phase bus" with "a second three-phase buffer," and replace the word "an" in Claim 6, line 3 with "and". Approval of the amendment is respectfully requested.

II. Claims Rejected Under 35 U.S.C. § 112

Claims 5-8 and 10-14 stand rejected under 35 U.S.C. § 112, second paragraph as being indefinite. Regarding Claims 5, 6, 10, 12, and 13, the Examiner asserts that the claimed "third", "fourth"...and "ninth" three-phase buffers imply that there are other three-phase buffers previous mentioned. Applicants submit that these claimed elements correspond to the three-phase buffers 403, 404...and 409 as shown in FIG. 3 of the Specification. Applicants use the "third", "fourth"...and "ninth" in the claims to clearly point out the correspondence of the claimed three-phase buffers in the claims and those described in the Specification. Renumbering the buffers in the objected Claims, as suggested by the Examiner, would destroy this correspondence. Moreover, these three-phase buffers (403-409) are independent of the first and second three-phase buffers (401,402). Designating these three-phase buffers (403-409) as the "third", "fourth"...and "ninth" three-phase buffers do not imply that they are dependent on or must coexist with a first and second three-phase buffers. Rather, the designation of these buffers is intended to be consistent with the designation in the supporting passages and figures in the Specification.

Claims 7, 8, 11, and 14 are objected to because of their dependence on Claims 5, 6, 10, 12, and 13. Thus, for at least the foregoing reasons, Applicants respectfully request the objections to Claims 5-8 and 10-14 are withdrawn.

III. Claims Rejected Under 35 U.S.C. § 102

Claims 1 and 9 stand rejected under 35 U.S.C. § 102(e) as being anticipated by U.S. Pre-Grant Patent Publication No. US 2001/0011353 issued to Little et al. ("Little"). Applicants respectfully traverse the rejection.

To anticipate a claim, the Examiner must show that a single reference teaches each of the elements of that claim. Among other elements, Claim 1 recites "an external access bus," "an internal access bus," and "an internal memory test bus," each of which is used for a different purpose. Little does not disclose three different buses. Rather, Little discloses a single bus structure (control bus/data bus 26) which is connected to the CPU, the memory, and the peripheral devices. Thus, every information bit transmitted between the CPU and the memory, or the CPU and the peripheral devices, is transmitted through the same single bus structure (control bus/data bus 26). The concept of three different buses are entirely absent in Little's disclosure.

In the Office Action, the Examiner divides control bus/data bus 26 into different sections and asserts that each of the sections teaches one of the claimed buses. However, a single bus cannot be artificially divided into different buses. Devices on the same bus are subject to the same electrical constraints and communication protocols while devices on different buses may not. Thus, it is inappropriate to equate a single bus to three different buses.

Moreover, control bus/data bus 26 taught by Little is different from any of the three claimed buses. Control bus/data bus 26 at most may be characterized as bus 210 connected to an external I/O, as shown in Applicants' FIG 3.

Accordingly, reconsideration and withdrawal of the anticipation rejection of Claim 1 are requested.

In regard to Claim 9, Claim 9 depends from Claim 1 and incorporates the limitations thereof. Thus, at least for the reasons mentioned above in regard to Claim 1, Little does not anticipate Claim 9. Accordingly, reconsideration and withdrawal of the anticipation rejection of Claims 1 and 9 are respectfully requested.

IV. Claims Rejected Under 35 U.S.C. § 103(a)

A. Claim 2 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Little in view of U.S. Patent No. 6,725,307 issued to Alvarez ("Alvarez"). Applicants respectfully traverse the rejection.

To establish a *prima facie* case of obviousness, the relied upon references must teach or suggest every limitation of the claim such that the invention as a whole would have been obvious at the time the invention was made to one skilled in the art. Claim 2 depends from Claim 1 and incorporates the limitations thereof. Thus, at least for the reasons mentioned above in regard to Claim 1, Little does not teach or suggest each of the elements of Claim 2.

The Examiner relies on Alvarez for disclosing a latch structure. However, Alvarez does not cure the defect of Little for failing to disclose the three different buses as recited in base Claim 1. Moreover, Alvarez discloses a distributed system for a multi-process system using a bused-based cache-coherence protocol. The latch structure in FIG. 6 is equivalent to a general bi-directional bus structure that is divided into an input pass and an output pass. There is nothing in the cited reference that mentions or suggests that the bi-directional structure connects an external access bus to an internal access bus. Accordingly, reconsideration and withdrawal of the obviousness rejection of Claim 2 are requested.

B. Claims 3, 5-8, 10-14 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Little in view of U.S. Patent No. 6,725,307 issued to Klaas ("Klaas").

Claims 3, 5-8, 10-14 depend from Claim 1 and incorporate the limitations thereof. Thus, at least for the reasons mentioned above in regard to Claim 1, Little does not teach or suggest each of the elements of these claims.

The Examiner relies on Klaas for disclosing tri-state buffers. However, Klaas does not cure the defect of Little for failing to disclose the three different buses as recited in base Claim 1. Klaas discloses a system on a chip including a high-speed peripheral bus. The databus of base Claim 1, by contrast, has an internal bus structure in which an external access bus and an internal access bus are embodied. Thus, the peripheral bus disclosed by Klaas does not teach or suggest the internal bus as claimed. Accordingly, reconsideration and withdrawal of the obviousness rejection of Claims 3, 5-8, 10-14 are requested.

CONCLUSION

In view of the foregoing, it is believed that all claims now are now in condition for allowance and such action is earnestly solicited at the earliest possible date. If there are any additional fees due in connection with the filing of this response, please charge those fees to our Deposit Account No. 02-2666.

Respectfully submitted,

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Dated: February 23, 2006

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CERTIFICATE OF MAILING:

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Mail Stop Amendment, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

Amber D Saunders 2/23/06

Amber D. Saunders Date